A Dual Controller APC Engine Used for CMP Applications

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Abstract – Chemical Mechanical Polishing (CMP) is used as a common semiconductor manufacturing process to planarize the wafer topology. Typical operating methodology requires that a Look Ahead Test wafer first be processed from the product lot and purposely underpolished to prevent scrapping that wafer. Post process metrology is then done and the proper process parameters are calculated for that specific lot. Prior to starting the balance of the product lot, the original Look Ahead Test wafer is repolished if it is out of control limits. This process is repeated for the next lot.

This methodology is labor intensive, prone to error and impacts the cycle time or Units per Hour (UPH) of this manufacturing process. Each of these factors contribute to degrading the efficiency of the CMP operation because more operators and tools are needed to produce the required quantity of material. Risk of a large margin of error exists when operators are allowed to manipulate recipe parameters, which can result in out of spec material that would need to be scrapped. An Advanced Process Control engine was developed that increased UPH while improving Cpk.

INTRODUCTION

Cypress Semiconductor Inc. utilizes a continuous improvement program to look for alternative ways to improve the efficiency of their operation. This largely means that the same tool set is required to operate to tighter specs with greater uptime and higher throughput. A dual controller APC engine has been developed by Cypress Semiconductor to target two specific areas of variability in the CMP operation. This controller has been fully integrated into the host automation and has both improved performance to target in both areas of interest as well as an increased UPH with decreased operator intervention.

ARCHITECTURE

An Advanced Process Control (APC) Engine was developed that is fully integrated between the CMP work cell, the Host Equipment Manager (EM) and the Manufacturing Execution System (MES) database environment. Refer to Figure 1. The CMP Work Cell consists of the polishing tool and thin film metrology. The CMP tool is an industry standard tool with little mechanical modification. This polisher has a single polish head that can process wafers on two separate polish pads. The insitu metrology tool is an after-market, commercially available, self-contained system that is physically located in the output area of the polisher. The insitu metrology measures wafer N while wafer N+1 is being polished. A standard PC serves as the EM for each component of the CMP work cell. This PC is networked to the MES. The MES database contains all required data to perform the calculations required to start the lot for processing.

The EM is responsible for lot and operator identification, recipe selection and material tracking. Refer to Figure 2. Since this is a Wet Processing tool, the product material is switched from the standard pod and cassette into dedicated CMP cassettes. The operator logs the lot into the CMP process step by scanning the lot ID barcode with a laser scan gun. This same scan gun is used by the Operator to scan their ID badge. These inputs are sequentially prompted by the EM and are automatically triggered with lot placement. After the lot identification is made, the EM does a “move in” function with the MES, which denotes this lot is active and in process on this polisher. This transaction is complete with a time stamp. Once lot identification has been done, the following data is retrieved from the MES for the target lot and tool combination.

Deposition Thickness

CMP Target, control limits and spec limits

Polish Rate for that tool

Base Recipe Identification

L2L Model Parameters

W2W Model Parameters

This data is subsequently delivered to the APC engine. When the lot is finished, all process data is sent to the MES database, which in turn calculates specific performance metrics and plots them on SPC charts. The EM finally performs a “move-out” transaction complete with a time stamp.

The APC Engine resides on the same PC as the EM. It is a separate program that runs in conjunction with the EM. The APC Engine consists of two separate controllers that automatically calculate the process parameters for specific scenarios. The first scenario is the feed forward Lot-to-Lot (L2L) case whereby lot based data, tool based data and

device characteristics are analyzed to determine optimum CMP recipe parameters. This is used to start the lot.

The other controller is the feed back Wafer-to-Wafer (W2W). This targets the reduction of any variability after the lot has been started. The W2W controller leverages the insitu CMP metrology and makes further recipe adjustments to compensate for any across the lot (W2W) variability. This controller reduces the combined W2W variability and does not attempt to discriminate between it's source, whether it be Polisher or Deposition Tool induced.

INTEGRATION

The Equipment Manager (EM) was developed in-house and is responsible for material and operator identification, recipe selection and process monitoring. The Advanced Process Control (APC) Engine was also developed in-house with all the statistical modeling being done by the staff engineering team. The entire project was integrated and deployed by the staff engineering team.

MODELING

The derived models were obtained by analyzing actual process data over a ninety day period. Ninety days was chosen to allow for all known variances to be included in the models. These variances included device to device, tool to tool, normal consumable changes and incoming batches from our suppliers. The analysis netted common modeling techinques[1,2] for calculating the polish rate of the tool and both the L2L & W2W controller parameters. The resultant models were further analyzed to produce optimal results by changing each term in their respective model and minimizing the delta to target.

Each controller had to comprehend the varying polish rates that accompany a CMP process. Refer to figure 3. There are two phases of the CMP polish process. The first phase is the non-linear region where polish rate decreases occur over time because the initial polish only affects the high areas of topography. As the wafer nears the planar state, the polish rate will stabilize and approximate a flat wafer polish rate. That is the linear polish phase. This varying rate will be device specific, whereby the line size and spacing as well as the amount removed, can effect the modeling. Each controller additionally had to compensate for both high and low volume devices. A high volume device is one that is run every day in quantity. A low volume device is one that is run once per quarter or less.

Once the lot has started the W2W controller starts and adjusts the polish time for each subsequent wafer. The previous wafer's delta from target is used by the W2W controller, which adjusts polish time based on the linear polish rate regime. The linear polish rate used for the W2W controller can be adjusted for each device family.

There are many parameters that influence polish rate for the oxide CMP system. To obtain a good control system the variability of each of these parameters must be reduced. This is done through a tool lockdown process. Any process that cannot be adequately controlled must be monitored and compensated for by the L2L control algorithm. One example of this is the incoming thickness of each production lot. This data is measured at the previous step and used as a factor to determine the lot polish time. Variations in the previous process step are eliminated from the process control equation because each lot is measured. Other sources of variation such as consumable life are controlled by the tool polish rate and are not individually measured.

The controllers have two outputs, overall polish rate and within wafer thickness variation. Many tool parameters are measured during the modeling process. These experiments determine the factors that affect polish rate or within wafer thickness variation. Once this data is known, the control algorithm is set up to adjust polish parameters to maximize the tool performance.

PERFORMANCE

The original performance improvement targets focused on eliminating the test wafer methodology and decreasing total variability. The actual performance results of this controller came in the following areas:

Performance results

Improved CpK. This was achieved by reducing both the L2L and W2W variances. A 45% reduction in the standard deviation was seen on the CMPM layer. This was seen across several devices and lots. CMPM is the intermetal dielectric polish step whereby the oxide is planarized over a high aspect ratio metal stack. A Multi-variate graph showing performance of wafer averages by run order, lot and device is shown in Figure 4. One can see how well each controller performed. The first wafer is on target and the balance of the lot is closer to target with respect to the uncontrolled (test wafer) methodology.

Increased UPH. Since the Test wafer was eliminated, the cycle time was decreased by about 25 minutes per lot. This netted an increase in UPH by 10% to 14% depending upon the total process time per step. This had significant impact by avoiding the purchase of additional CMP tools. For a typical fleet of 10 tools, we gained one full tool of capacity.

Engineering efficiency due to recipe elimination. The EM does 'base recipe' selection and the APC engine sets the process parameters for each lot. The total recipe count on the polisher went down from ~40 recipes to 3 'base' recipes.

Increased Efficiency. Operator efficiency was greatly improved due to the elimination of the labor intensive "test wafer" methodology. This allows the same fleet of tools to be operated with less headcount.

Line Yield Improvement. Since the Operator was not selecting, calculating or setting the recipe parameters, common areas of human error were removed. Line yield improved moderately.

New Capital Avoidance. Equipment lifetime was extended by reducing the total variability allowing the same fleet of polish tools to meet specifications for the next technology node. Technology evolution typically reduces the specification limits by 7-14% from one technology node to the next. When Cpk was improved by 0.4, the current tool set could then meet the requirements for the next node. Refer to Figure 5.

PROCESS MONITOR

Since there are two specific controllers involved, a specific monitoring and control methodology[3] was created. The MES Statistical Process Control (SPC) system was utilized by changing the data collection scheme. Two charts are in use each targeting one controller. Refer to Figure 6. The first chart monitors the L2L controller performance by plotting the X_{bb} of all raw data for the first two wafers only. This is normalized and presented as a Delta to Target or D2T. The second chart monitors the W2W controller by plotting the sigma of the wafer means for wafers #5 through #25. By ignoring the first 4 wafers of a 25 wafer lot, any ringing effects from the L2L controller are removed from the W2W monitor. Standard control limits and rules are in place.

CONCLUSION

An Advanced Process Control Engine was successfully developed and deployed on the CMP work cell. This controller was integrated with the automation host controller, the main data base, polish tool and insitu metrology. The success came in several areas all improving the operational efficiency of the CMP operation. Improved Cpk and increased UPH were by far the leading responses. Decreased human intervention also contributed to the success of this project.

FUTURE WORK

Original work targeted two specific sources of variation. Future work will be done to include a controller to target within wafer (WIW) variances. This will be done in conjunction with the added capability of Fault Detection software.

REFERENCES

[1] David Drain. *Statistical Methods for Industrial Process Control.* Chapman & Hall, 1997, ch 2&3, pp 116-219.

[2] Box & Luceno. *Statistical Control by Monitoring and Feedback Adjustment.* Wiley Interscience, 1997, ch 4-5 & 12, pp 85-127,269-295.

[3] David Drain. *Statistical Methods for Industrial Process Control.* Chapman & Hall, 1997, ch 5&6, pp 282-381.

AUTHORS BIOGRAPHY

Gregg Robinson is a Sr. Process Engineer at Cypress Semiconductor Minnesota Inc. He has a Masters degree in Manufacturing Systems Engineering and a bachelors degree in Materials Science from the University of Minnesota. Gregg is currently working in the CMP manufacturing area of Cypress Semiconductor Minnesota Inc., and has been with Cypress since 1993.

Gene Smith is a senior member of technical staff where he has recently been developing and deploying FDC and APC projects at Cypress Semiconductor Minnesota Inc. Before that, he was an R&D Process Engineer developing next generation processes on various etch and diffusion equipment. Gene has been employed by Cypress Semiconductor Inc since 1984.

Figure 1

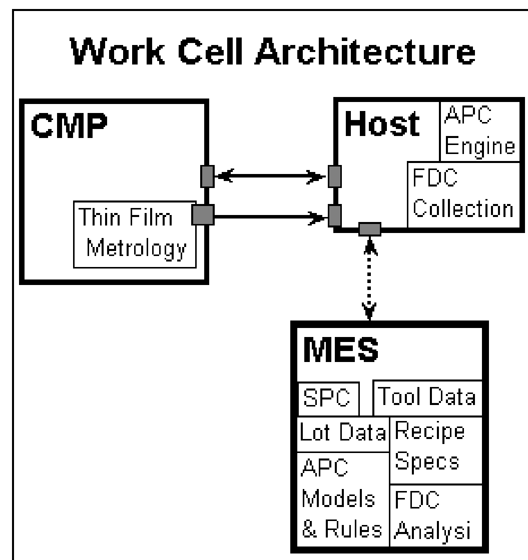

Figure 2

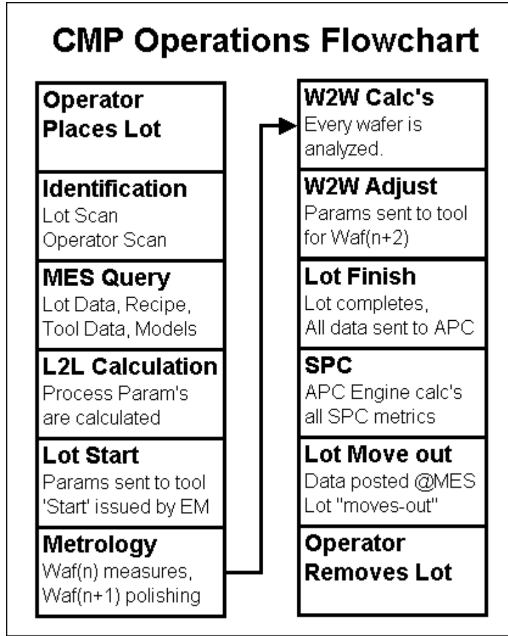

Figure 3

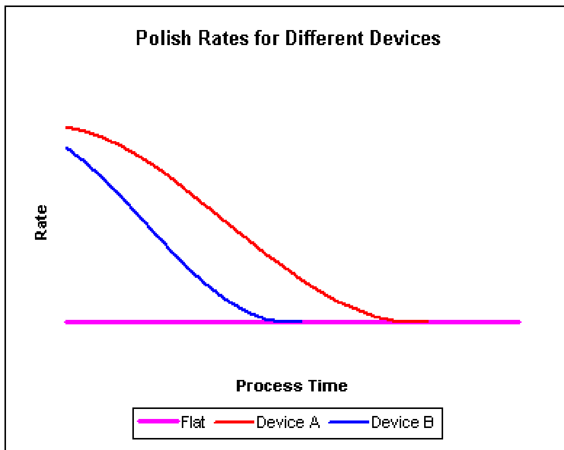

Figure 4

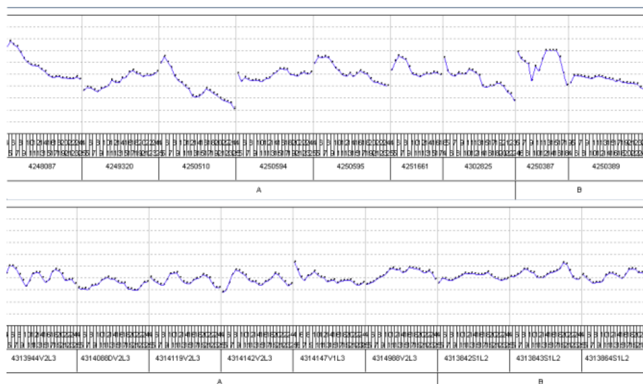

Figure 5

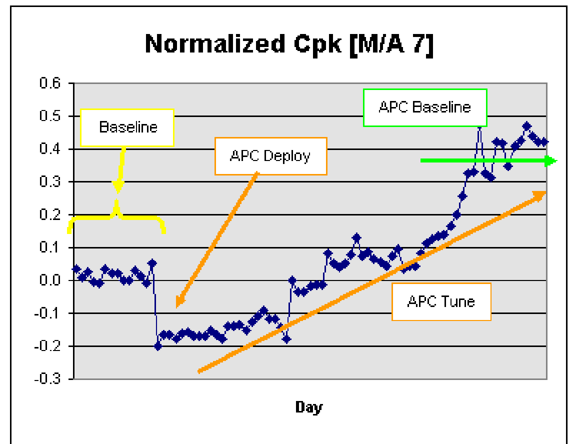

Figure 6