Simple Implementation of a First Order Advanced Process Control Engine For Thin Film Applications

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Abstract – PECVD of dielectric films show two major variation sources (lot-to-lot variation and device-to-device variation) that reduce the process Cpk and increase the cost of operation. To improve the PECVD process manufacturability, some form of automated compensation at runtime is necessary. This paper presents a First Order APC Engine that compensates for process tool deposition rate drift and pattern density differences. Both are needed to allow for a single recipe to deliver 'on target' performance for many devices and process tools. This project improved Cpk from ~1.0 to over 2.0.

INTRODUCTION

PECVD thin film deposition is a common process used to deposit dielectric thin films, both in the front end and back end of line during semiconductor wafer processing [1]. These dielectric films are used as etch stops, inter-layer dielectric, passivation layers, etc. The thickness of these dielectric films needs to be controlled within a tolerance so that the critical dimensions (such as gate length, contact & via width) meet device specifications.

PROCESS VARIATION

Two major sources of variation that contribute to Cpk failure in manufacturing are lot-to-lot (L2L) and device-to-device (D2D) variation. The D2D variation in film thickness is due to pattern density effect (see Figure 1), also known as the loading effect [2].

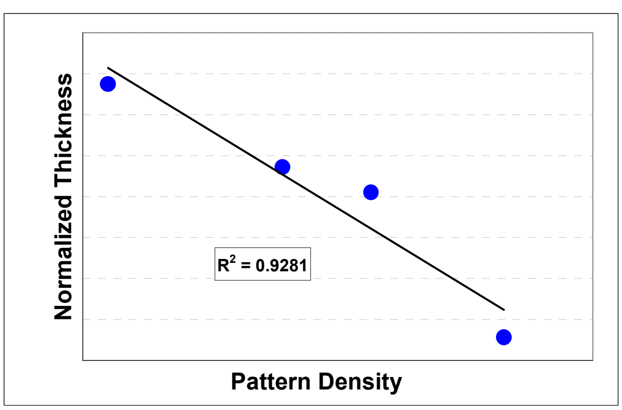

Figure 1: Device to device (D2D) variation is due to difference in pattern density of incoming mask layer as shown by change in normalized thickness vs. pattern density

Different devices use different reticles and hence have different pattern density. Typical PECVD processes used in semiconductor fabrication are mass transport limited. Hence, these factors lead to a difference in thickness between devices when using the same deposition process. To target the same thickness for different devices, multiple recipes need to be created and maintained.

The L2L variation arises due to drift of the film deposition rate through tool use. After a tool wet-clean, the residual dielectric build-up in the reactor is negligible. But with increasing tool use and increasing wafer counts, especially when using a broad product mix (such as different dielectric film processes in same tool), the residual dielectric builds up in the reactor. This causes the process deposition rate to drift as shown in Figure 2. The deposition rate drift necessitates that frequent quals be done to keep the process recipe on target.

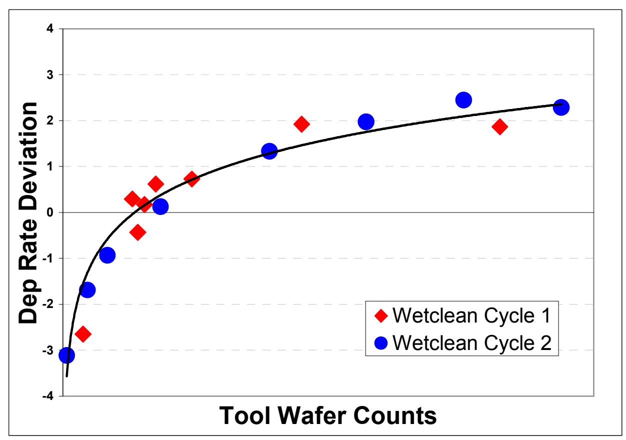

Figure 2: Lot to lot (L2L) drift is due to drift in the tool deposition rate after a wet clean with increasing wafer count/tool use.

Using different recipes for different devices requires managing multiple recipes that is costly, error-prone, time consuming and lowers throughput and Cpk. To extend the current dielectric PECVD tools for 90nm technology and beyond, we needed to reduce the variation sources. To enable cost-effective six-sigma manufacturing and to extend tool life, we are using an advanced process control (APC) Engine for PECVD thin film deposition.

This project targeted the automatic compensation at run time, of the two largest sources of variation – L2L and D2D. The APC Engine is a "single input, single output"

(SISO) type, which makes the controllers easy to develop internally and enhance when required. This approach avoided costly 3rd party APC solutions that weren't required for this level of control.

SYSTEM ARCHITECTURE

A Remote Host [3] is utilized to interface both the PECVD reactors and the metrology tools with the Manufacturing Execution System (MES) as shown in Figure 3. This host runs on a standard PC that is networked to the MES and connected directly to the process and metrology tools with a serial connection using the semiconductor standard SECS/GEM protocol. This Host is written with a commercially available software package that allows for end user customization. The Host also supports an array of applications including a commercially available Lot Scheduler and Fault Detection applications along with internally developed SPC and WIP Tracking applications. The Host is also a single point of contact for the Operator. All communications between the Host and MES are done with a proprietary dynamically linked library (DLL).

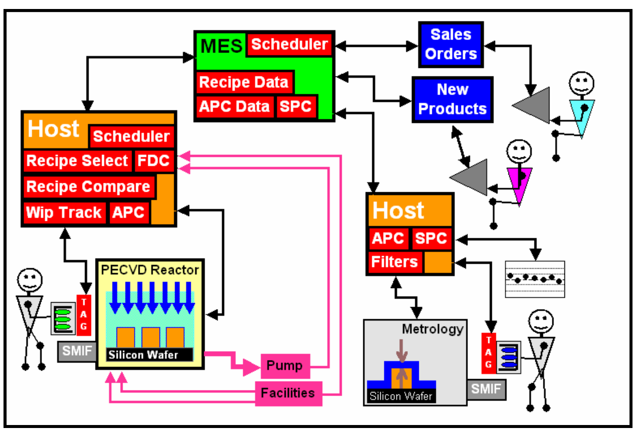

Figure 3: Host & MES System Architecture with both Process & metrology tools shown along with off-FAB inputs.

When the Operator places a lot on the SMIF port of the process tool, the Host reads the electronic lot identifying tag and Operator Badge scan, then performs the usual Lot Tracking functions. The Host then retrieves the device number, thickness target, and all APC controller data from the MES. These calls, checks and calculations take only a few seconds.

APC ENGINE

The APC engine logic resides within Host code with all the data in the MES. After all the data is retrieved as described earlier, the APC engine performs several calculations as well as comparing tool and device state data to certain business rules. These business rules are items like how far into the preventative maintenance cycle is the reactor or how much use has the reactor has seen since the last time this specific recipe was processed. The APC can reject a lot if any of these items do not meet these business requirements.

The Tool Controller works with the feedback of normalized data and is used as a monitor of the reactor state as seen in Figure 4. One can see that this normalized data shows tool process rate drift and how it is perturbed when chamber preventative maintenance functions are performed. The flat wafer or test qualification (QUAL) deposition rate data and the normalized process rate (NPR) from the most recent product lots are both analyzed. The Host compares the date of each and selects the newest data set. This allows the tool controller to be reset upon a passing QUAL run while leveraging all product data on a single Tool/base recipe SPC chart.

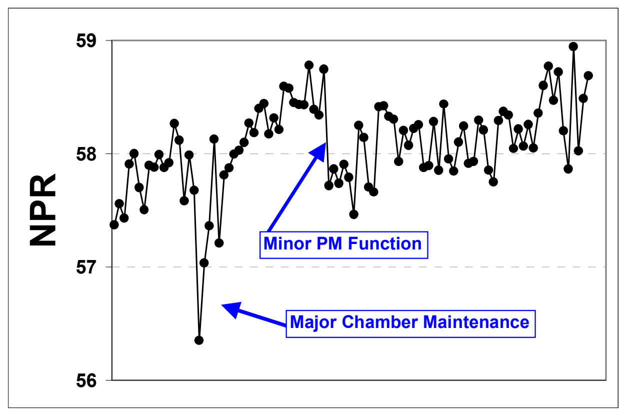

Figure 4: Normalized Process Rate chart for one tool, one process and 9 devices showing the impact on deposition rate that PM functions have.

Simple statistical calculations are performed on the NPR & QUAL data to estimate [4] the NPR for run (n+1). This information is used to calculate the station dep time (SDT) and is posted to an SPC chart where standard violation rules are in place.

The Device Controller compensates for varying device differences and serves as the feed forward component [5] to our APC Engine. This simply is a ratio of this specific device deposition rate to the specific flat wafer QUAL rate and is designated 'device-layer-coefficient' or DLC. The number of times a specific device has been processed is also kept track of. This is to allow for the following logic to handle new devices more efficiently without perturbing the tool controller. Typically the gain of this controller is very low after a few runs have been processed but very high for the first few lots. When new products are introduced to the FAB, Host logic and specific business rules were developed to have the Design community enter details about a specific device and layer directly into the MES via an intranet web page. Previous methodology was to process a QUAL wafer with one product wafer then measure them both. This took significant time since the tool is a batch reactor and there wasn't an existing metrology recipe, all of which was prone to error.

After the DLC(n) has been retrieved, it is used along with the NPR(n) to make the calculations for the SDT. The Host then selects the process recipe and sets the SDT to the output of the APC Engine. The lot is then started by the Host issuing the "start" function using standard SECS/GEM commands.

When the processed lot is sent to metrology, the Operator places the lot, the Host reads the electronic identification tag, Operator Badge scan and performs all the Lot Tracking functions. The DLC error term is established [5] and fed into the controller to calculate the DLC value for the (n+1) lot. The NPR error term [4] is also established and posted to the SPC environment ready for use to estimate the NPR(n+1) value for the next process run. If the NPR value is below certain control limits, the MES would automatically down the Process tool preventing the processing of additional material.

Previous SPC methodology plotted a single device on a single SPC chart. Figure 5 shows two device charts overlaid in run order with the PM events highlighted.

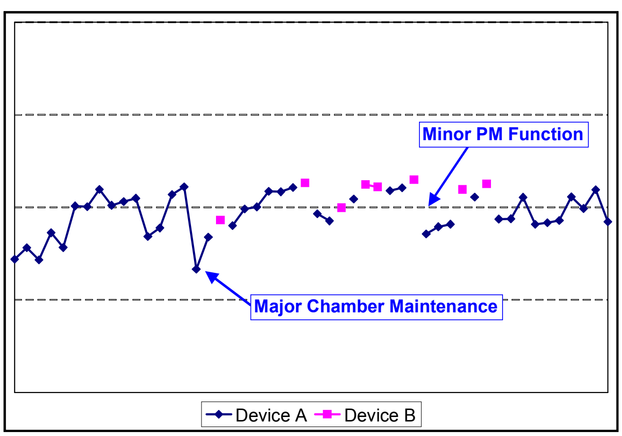

Figure 5: Two Device Based SPC charts overlaid. If Device B chart used to control the tool, PM events would have been missed

The chamber maintenance functions don't distinguish themselves as well as Figure 4 because the total number of data points is much less. Should tool control be done with the Device B chart, the PM events would have been completely missed. Tool control sensitivity must not be gated to product mix and is alleviated with the NPR scheme.

Several data filters are active at either the Host level or the MES level and prevent suspicious data from erroneously perturbing either controller. The rule here is that "no data is better than bad data". The SPC package serves as the visual interface with the traditional 'run stop' rules to the operators on the floor. The latter application augments the Process Engineer's toolbox by providing precision data for process tool lockdown purposes.

RESULTS

The entire system was implemented into a volume Mfg. environment with relatively minimal (but consistent) effort and for no capital dollars. The time to model this reactor's control requirements and develop the Host Code was actually shorter than the time it took to determine what the business rules and operational scenarios for this specific reactor were. Since the APC engine was developed internally, as we learn, changes and enhancements can be quickly implemented without additional capital dollars.

The benefits of this project were many. The Delta to target (D2T) improvement as seen in Figure 6 shows that after deployment the tuning is getting better over time.

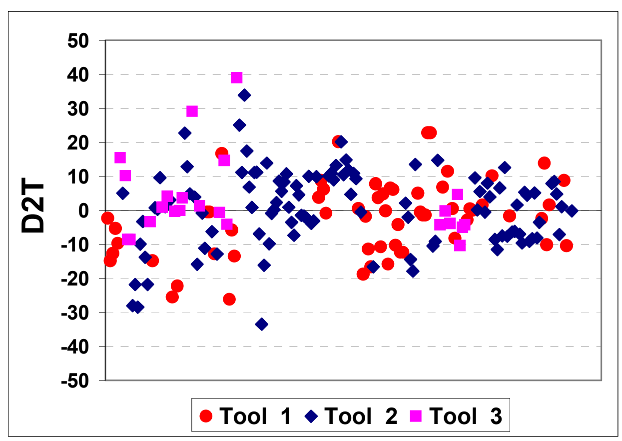

Figure 6: Delta to Target for 3 tools, 2 layers and 9 devices

This was due to the initial deployment of the APC Engine across the tool fleet and device base, and was expected.

The sources of variation [6] and the Cpk improvement for the project are shown in Figure 7.

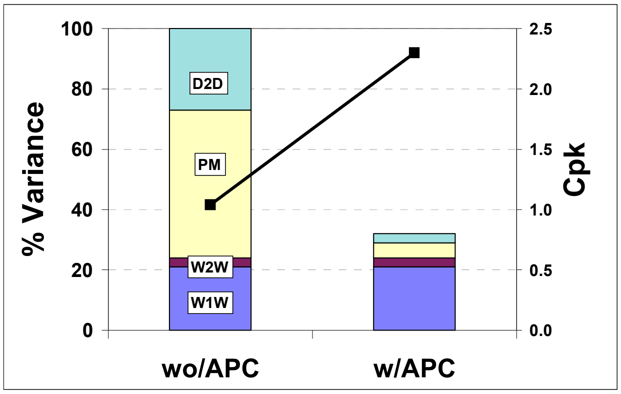

Figure 7: Sources of variation and Actual Cpk Improvement

The recipe administration was significantly reduced as a single 'base' recipe would support the entire product mix which then allowed the reactor to support fewer process recipes. Significant human error at the process sustaining level was in turn eliminated. Tool control is now independent of device-to-device differences, which allows for significantly higher signal to noise ratio in the SPC database. Many device based SPC charts were combined into NPR charts that posted every lot to a single chart. So reactor trending is seen much earlier and action can be taken far sooner than before as seen in Figure 4. The auto DLC entry of new device data eliminated ~6 hours per layer of cycle time. This allowed the FAB to deliver first silicon far quicker than ever before. The data filters kept the data base homogenized and prevented unexpected excursions on subsequent batches. Finally, since every lot was posted to a tool based SPC chart, the QUAL frequency was reduced.

CONCLUSIONS

Typical wafer fabrication process tools have several sources of variation and if properly understood, cost-effective solutions such as the SISO APC controller can be developed to address these variation sources. Benefits are not limited to Cpk, but include fewer human errors while enabling better tool control and extended the tool life. Since this controller is internally created, it can be integrated quickly to other process tools.

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AUTHOR BIOGRAPHY

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